Code No: 153AG **R18**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, December – 2024/January -2025
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, CSBS, CSIT, CE(SE), CSE(CS), CSE(AI&ML), CSE(DS), CSE(N), AI&DS, AI&ML, CSD)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A
(25 Marks)

1.a)	Draw block diagram of digital computer.	[2]
b)	What is instruction cycle?	[3]
c)	What is control unit?	[2]
d)	What are one address instructions?	[3]
e)	What are non numeric data types?	[2]
f)	What is the significance of 1's complement?	[3]
g)	What is auxiliary memory?	[2]
h)	Explain about input-output interface.	[3]
i)	List out CISC Characteristics.	[2]
j)	What is cache coherence?	[3]

PART – B
(50 Marks)

2. Explain logic and shift micro operations with examples. [10]

OR

3.a) Explain arithmetic logic shift unit.
b) List and explain various instruction codes. [5+5]

4. Explain about two address and three address instructions. Give examples. [10]

OR

5. Explain immediate addressing mode and register mode with examples. [10]

6. Explain floating point representation in detail. [10]

OR

7. Explain Booth multiplication algorithm with an example. [10]

8. Explain direct memory access in detail. [10]

OR

9. Explain about memory organization. [10]

10.a) Explain about RISC pipeline
b) Elaborate on interprocessor arbitration. [5+5]

OR

11.a) Explain about vector processing.
b) Elaborate on interprocessor communication and synchronization. [5+5]

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